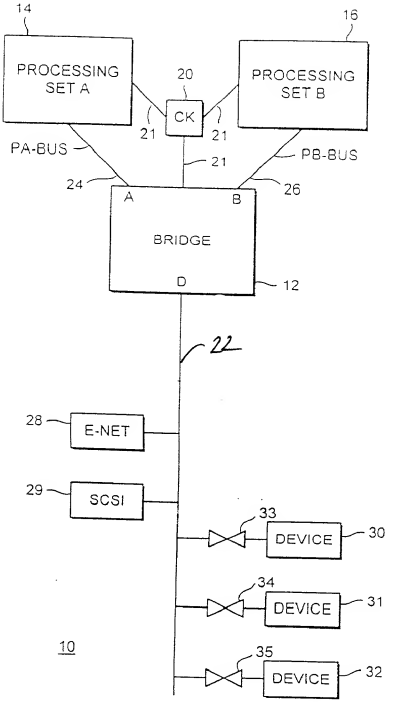
14
16
PROCESSING SET A
20
PROCESSING SET B
CK
21
21
PA-BUS
21
PB-BUS
24
26
A
B
BRIDGE
D
12
22
28
E-NET
29
SCSI
33
DEVICE
30
34
DEVICE
31
10
35
DEVICE
32

FIG. 1

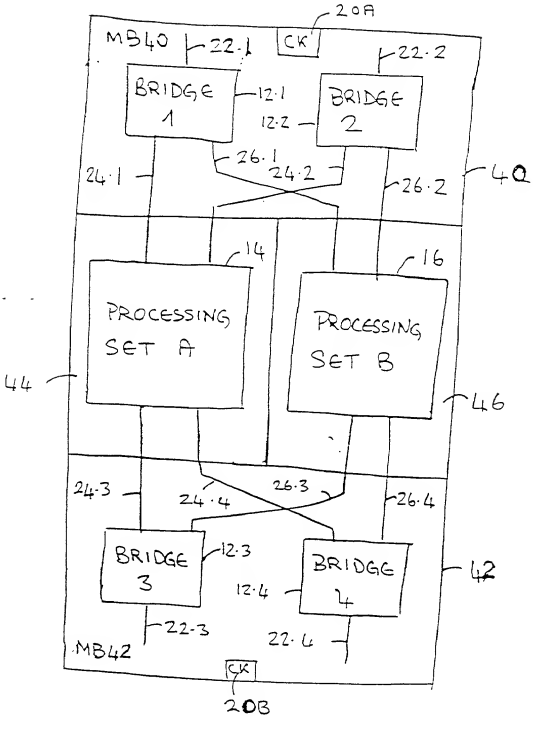
20A
MB40
22.1
CK
22.2
BRIDGE 1
12.1
BRIDGE 2
12.2
26.1
24.1
24.2
26.2
40
14
16
PROCESSING SET A
PROCESSING SET B
44
46
24.3
24.4
26.3
26.4
BRIDGE 3
12.3
BRIDGE 4
12.4
42
22.3
22.4
MB42
CK
20B

FIG. 2

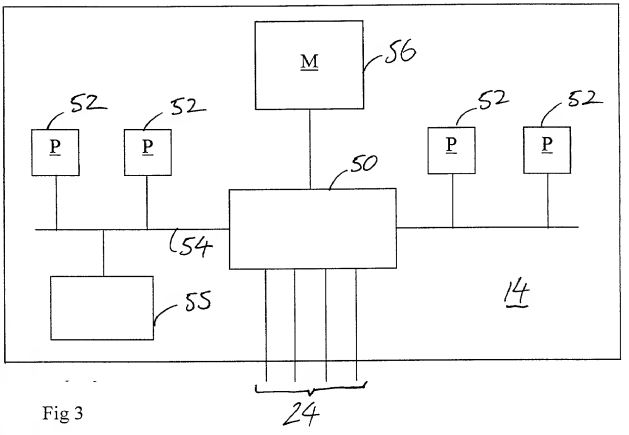

Fig 3

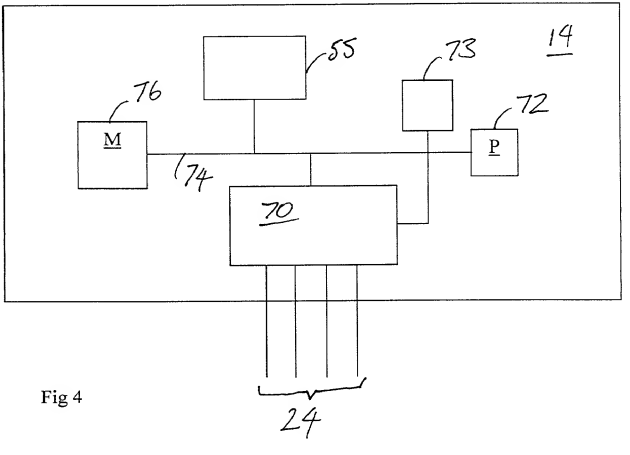

Fig 4

Bits	Field	Use	RW
<63:48>	*manuf*	Manufacturer identification	R
<47:32>	*impl*	Implementation identification	R
<31:24>	*mask*	Mask set version	R
<23:16>	*Reserved*	—	R
<15:8>	*maxtl*	Maximum trap level supported	R
<7:5>	*Reserved*	—	R
<4:0>	*maxwin*	Maximum number of windows of integer register file.	R

Fig 5

09/521,760 03/09/2000

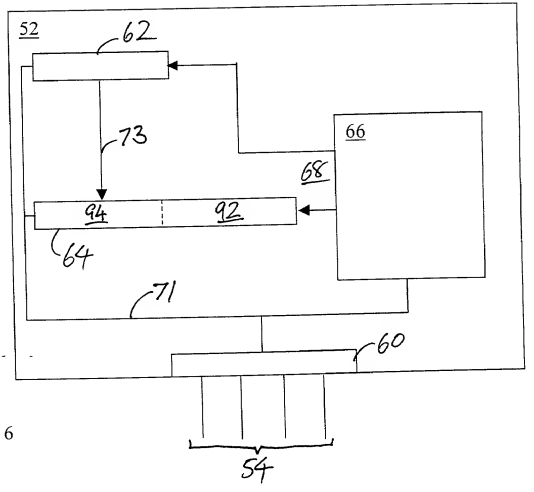

Fig 6

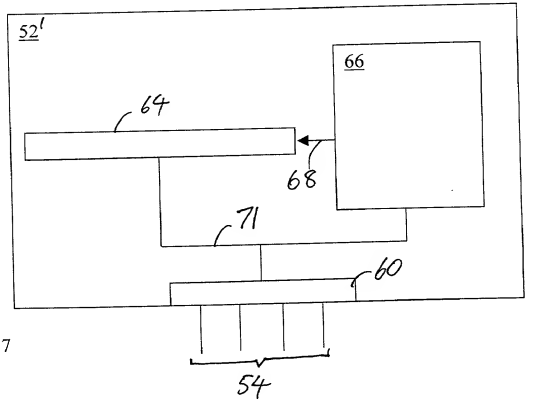

Fig 7

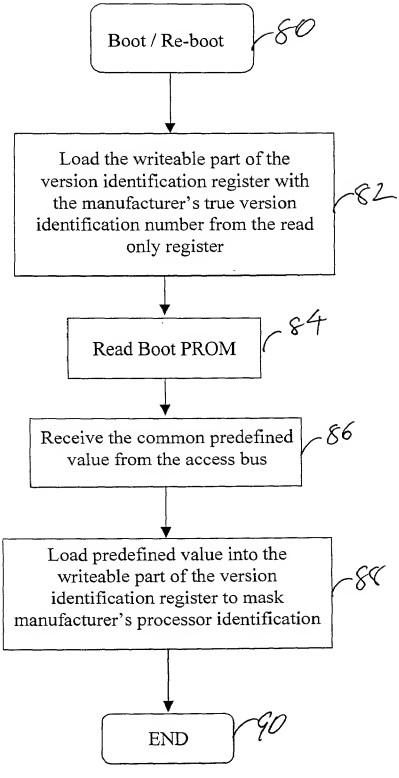
Boot / Re-boot
80
Load the writeable part of the version identification register with the manufacturer's true version identification number from the read only register
82
Read Boot PROM
84
Receive the common predefined value from the access bus
86
Load predefined value into the writeable part of the version identification register to mask manufacturer's processor identification
88
END
90

Fig 8